Code No: RT22054 **R13** SET - 1

II B. Tech II Semester Regular Examinations, May/June - 2015
COMPUTER ORGANIZATION
(Com. to CSE, IT, ECC)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART-A

1. a) Find (1001101 - 10101001) using 1's complement?
   b) What is instruction cycle?
   c) Write the advantage of RISC over CISC?
   d) Draw the circuit diagram and Truth table for Full adder?
   e) Draw the hierarchy of memory? Why memory hierarchy is important in computer system?
   f) Differentiate between Synchronous and Asynchronous modes of data transfer?
   (3M+3M+4M+4M+4M+4M)

PART-B

2. a) Discuss three representations of Signed integers with suitable examples.
   b) Explain the components of the Computer system. (8M+8M)

3. a) List and explain the steps involved in the execution of a complete instruction
   b) What is Micro operation? Briefly explain the arithemetic micro operations? (8M+8M)

4. a) Explain the organization of registers.
   b) Explain how microinstructions execution takes place. (8M+8M)

5. a) Explain the issue involved with multiplication operation.
   b) Design 4-bit adder/Subtractor and explain its function. (8M+8M)

6. What is a mapping function? What are the ways the cache can be mapped? Explain in detail. (16M)

7. a) What is multiprocessor system? Explain the advantages of multi processors over uniprocessors
   b) Explain the functions of typical input-output interface. (8M+8M)

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Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART-A

1. a) What are 2's Compliment? Give its Significance?
   b) What is interrupt? Give the steps for handling interrupt?
   c) Compare RISC and CISC?
   d) Realize full adder using two half adders and logic gate?
   e) What is Auxiliary memory?
   f) What are different forms of parallelism? (4M+4M+4M+4M+3M+3M)

PART-B

2. a) Explain the functional architecture of the computer system.
   b) Discuss the concept of compliments used to represent signed numbers. (8M+8M)

3. a) What is instruction cycle? Briefly explain with the help of state diagram?
   b) Briefly explain the arithmetic logic shift unit (8M+8M)

4. a) Explain the various addressing modes with examples.
   b) Explain the basic organization of microprogrammed control unit (8M+8M)

5. a) Design carry look ahead adder and explain its function.
   b) Derive and explain an algorithm for adding and subtracting 2 floating point binary numbers (8M+8M)

6. a) Explain the Address Translation in Virtual Memory
   b) Explain different types of mapping functions in cache memory (8M+8M)

7. a) How data transfers can be controlled using handshaking technique?
   b) Explain organization of multiprocessor system with neat sketch. (8M+8M)

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Code No: RT22054 **R13** SET - 3

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Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART-A

Part A

1. a) What is parity? Give its significance?
   b) What is one address, two address and three address instruction formats?
   c) What is Register Indirect Addressing mode? Give an example?
   d) Draw the circuit diagram and Truth table for half adder?
   e) What is Cache memory? Mention its advantages?
   f) What is the use of priority interrupt? (3M+4M+4M+4M+4M+3M)

PART-B

2. a) Describe the connections between the processor and memory with a neat structure diagram
   b) Find 2's complement of the following
   i) 10010 ii) 111000 iii) 0101010 iv) 111111 (8M+8M)

3. a) Explain the Memory reference instructions? Give examples?
   b) List and explain the shift micro operations? (8M+8M)

4. a) Explain micro instruction sequencing in detail.
   b) With a neat diagram explain the internal organization of a processor. (8M+8M)

5. a) Explain hardware implementation of Binary multiplier with example.
   b) Discuss decimal arithmetic operations (8M+8M)

6. a) Explain about associative memory
   b) Explain internal organization of memory chips. (8M+8M)

7. a) With a neat sketch explain the working principle of DMA
   b) Explain the interconnection structure for multiprocessor systems (8M+8M)

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Code No: RT22054 **R13** SET - 4

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Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART-A

1. a) What Sign magnitude representation? Give an example?
   b) Draw the structure of basic computer system?
   c) What is addressing mode? List any four Addressing modes?
   d) Draw the diagram for 4-bit adder?
   e) What is Virtual memory? Why it is significant?
   f) What is DMA? Write its Advantages? (4M+3M+4M+3M+4M+4M)

PART-B

2. a) Discuss about fixed point and floating point representations
   b) What are functions of ALU and explain. (8M+8M)

3. a) What is RTL? Explain with suitable examples? What is its significance Instructions?
   b) What is Interrupt? Explain Input output interrupts? (8M+8M)

4. a) Explain different addressing modes.
   b) Mention the advantages and disadvantages of microprogrammed control hardwired control (8M+8M)

5. a) Explain division algorithm with example.
   b) Explain Booth Multiplication algorithm with example. (8M+8M)

6. a) Analyze the memory hierarchy in terms of speed, size and Cost.
   b) Design 64k X 16 memory chip using 16k X 8 memory chips (8M+8M)

7. a) What are handshaking signals. Explain the handshake control of data transfer during input and output operation
   b) What is parallel processing? Explain any parallel processing mechanism. (8M+8M)

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